WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first gate insulating film formed in a first active region of a semiconductor substrate and having a first film thickness; and

a second gate insulating film formed in a second active region of said semiconductor substrate and having a second film thickness smaller than the first film thickness,

wherein a surface of the semiconductor substrate in the first active region is lower than that in the second active region.

2. The device according to claim 1,

wherein the semiconductor substrate surface in the first active region is lower than that in the second active region by an amount corresponding to a difference between the first and second film thicknesses, so a surface height of said first gate insulting film is substantially equal to that of said second gate insulating film.

3. The device according to claim 1,

wherein the first and second active regions are isolated by a trench filled with an insulating film, and

a gate electrode is formed on each of said first and second gate insulating films.

4. The device according to claim 3,

wherein said gate electrodes on said first and second gate insulating films are made of the same material and have substantially the same thickness.

5. A semiconductor device comprising:

a first gate insulating film formed in a first active region of a semiconductor substrate and having a

first film thickness;

a second gate insulating film formed in a second active region of said semiconductor substrate and having a second film thickness smaller than the first film thickness; and

a trench element isolation insulating region formed between the first and second active regions,

wherein a first height which is a surface height of said semiconductor substrate in the first active region on a bottom surface of the trench element isolation region is lower than a second height which is a surface height of said semiconductor substrate in the second active region on the bottom surface of the trench element isolation region.

6. The device according to claim 5,

wherein a difference between the first and second film thicknesses is 1/2 to twice a difference between the first and second heights.

7. A method of fabricating a semiconductor device comprising a first gate insulating film formed in a first active region of a semiconductor substrate and having a first film thickness, and a second gate insulating film formed in a second active region of the semiconductor substrate and having a second film thickness smaller than the first film thickness, comprising:

processing a surface portion of the semiconductor substrate such that a semiconductor substrate surface in the first active region is lower than that in the second active region.

8. The method according to claim 7,

wherein when the surface portion of the semiconductor substrate is processed, the semiconductor

substrate surface in the first active region is made lower than that in the second active region by an amount corresponding to a difference between the first and second film thicknesses, to make a surface height of the first gate insulting film substantially equal to that of the second gate insulating film.

9. A semiconductor device fabrication method comprising:

forming a mask which exposes a surface of a first active region and covers a second active region of a semiconductor substrate;

forming a first oxide film on the surface of the first active region by oxidation by using the mask;

removing the mask and first oxide film to make a semiconductor substrate surface in the first active region lower than that in the second active region;

forming a second oxide film on the surfaces of the first and second active regions;

leaving a portion of the second oxide film which exists in the first active region and removing a portion of the second oxide film which exists in the second active region; and

forming a third oxide film thinner than the second oxide film on a surface of the second oxide film in the first active region of the semiconductor substrate, and forming a fourth oxide film having a film thickness substantially equal to that of the third oxide film on the surface of the second active region,

wherein a first gate insulating film including the second and third oxide films is formed in the first active region, a second gate insulating film including the fourth oxide film in the second active region, and a surface height of the first gate insulating film is substantially equal to that of the second gate insulating film.

10. The method according to claim 9, further comprising:

depositing a first film made of a conductive material on the third and fourth oxide films, and depositing a second film serving as a polishing stopper on the first film;

patterning the first and second films into an electrode shape in the first and second active regions, and forming a trench in a surface portion of the semiconductor substrate in an element isolation region between the first and second active regions;

depositing an insulating film on an entire surface;

planarizing the insulating film by using the second film as a polishing stopper;

etching the insulating film in the element isolation region to decrease a height of the insulating film;

removing the second film;

depositing a third film made of a conductive material on an entire surface; and

patterning the third film into an electrode shape in the first and second active regions.

11. A nonvolatile semiconductor memory comprising a memory cell array and peripheral circuit,

wherein a transistor included in said peripheral circuit has a first gate insulating film formed in a first active region of a semiconductor substrate and having a first film thickness,

a transistor included in said memory cell array has a second gate insulating film formed in a second active region of said semiconductor substrate and having a second film thickness smaller than the first film thickness, and

a semiconductor substrate surface in the first active region is lower than that in the second active region.

12. The memory according to claim 11,

wherein the semiconductor substrate surface in the first active region is lower than that in the second active region by an amount corresponding to a difference between the first and second film thicknesses, so a surface height of said first gate insulating film is substantially equal to that of said second gate insulating film.

13. The memory according to claim 11,

wherein the first and second active regions are isolated by a trench filled with an insulating film, and

on each of said first and second gate insulating films, a floating gate electrode, interpoly dielectric film, control gate electrode, and control gate resistance decreasing metal film are formed.

14. The memory according to claim 11,

wherein in said memory cell array, a plurality of memory cell transistors are connected in series such that adjacent transistors share a source and drain, and selection transistors are arranged on two sides of said plurality of memory cell transistors.

15. A nonvolatile semiconductor memory comprising a memory cell array and peripheral circuit,

wherein a transistor included in said peripheral circuit has a first gate insulating film formed in a first active region of a semiconductor substrate and having a first film thickness,

a transistor included in said memory cell array has a second gate insulating film formed in a second

active region of said semiconductor substrate and having a second film thickness smaller than the first film thickness, and

on a bottom surface of a trench element isolation insulating region formed between the first and second active regions, a first height of a surface of said semiconductor substrate in the first active region is lower than a second height of the surface of said semiconductor substrate in the second active region.

16. The memory according to claim 15,

wherein in said memory cell array, a plurality of memory cell transistors are connected in series such that adjacent transistors share a source and drain, and selection transistors are arranged on two sides of said plurality of memory cell transistors.

17. A method of fabricating a nonvolatile semiconductor memory comprising a memory cell array and peripheral circuit,

wherein a transistor included in the peripheral circuit has a first gate insulating film having a first film thickness in a first active region of a semiconductor substrate, and,

a transistor included in the memory cell array has a second gate insulating film having a second film thickness smaller than the first film thickness in a second active region of the semiconductor substrate, and

the method comprises, processing a surface portion of the semiconductor substrate such that a surface of the semiconductor substrate in the first active region is lower than that of the semiconductor substrate in the second active region.

18. The method according to claim 17,

wherein the surface of the semiconductor substrate

in the first active region is lower than that of the semiconductor substrate in the second active region by an amount corresponding to a difference between the first and second film thicknesses, so a surface height of the first gate insulating film is substantially equal to that of the second gate insulating film.

19. The semiconductor device,

wherein an electronic card comprises the nonvolatile semiconductor memory set forth in claim 11.

20. An electronic apparatus comprising:

a card interface;

a card slot connected to said card interface; and

an electronic card capable of being electrically connected to said card slot,

wherein said electronic card comprises the nonvolatile semiconductor memory set forth in claim 11.

21. The semiconductor device,

wherein an electronic card comprises the nonvolatile semiconductor memory set forth in claim 15.

22. An electronic apparatus comprising:

a card interface;

a card slot connected to said card interface; and

an electronic card capable of being electrically connected to said card slot,

wherein said electronic card comprises the nonvolatile semiconductor memory set forth in claim 15.

23. The apparatus according to claim 20,

wherein said electronic apparatus is a digital still camera.

24. The apparatus according to claim 20,

wherein said electronic apparatus is a video camera.

25. The apparatus according to claim 20, wherein said electronic apparatus is a television.

26. The apparatus according to claim 20, wherein said electronic apparatus is an audio apparatus.

27. The apparatus according to claim 20, wherein said electronic apparatus is a game apparatus.

28. The apparatus according to claim 20, wherein said electronic apparatus is an electronic musical instrument.

29. The apparatus according to claim 20, wherein said electronic apparatus is a cellular phone.

30. The apparatus according to claim 20, wherein said electronic apparatus is a personal computer.

31. The apparatus according to claim 20, wherein said electronic apparatus is a personal digital assistant.

32. The apparatus according to claim 20, wherein said electronic apparatus is a voice recorder.

33. The apparatus according to claim 20, wherein said electronic apparatus is a PC card.